

ABSTRACT OF THE DISCLOSURE

In a method for manufacturing a single electron memory device including a single electron storage element in a gate lamination pattern formed on a nano-scale channel region of a MOSFET, formation of the gate lamination pattern includes sequentially forming a lower layer and a single electron storage medium for storing a single electron tunneling through the lower layer on a substrate, forming an upper layer including a plurality of quantum dots on the single electron storage medium, forming a gate electrode layer on the upper layer to be in contact with the plurality of quantum dots, and patterning the lower layer, the single electron storage medium, the upper layer, and the gate electrode layer, in reverse order.